(12) UK Patent Application (19) GB (11) 2 202 702 (13) A

(21) Application No 8707353

(22) Date of filing 27 Mar 1987

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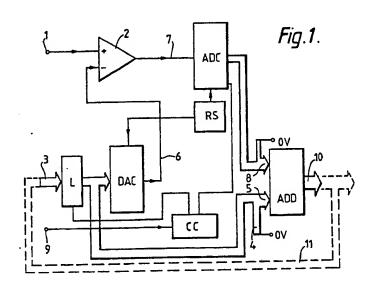
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(51) INT CL⁴
H03M 1/46

(52) Domestic classification (Edition J):
H3H 1X 2B 2G AB AU AV
U1S 2167 2204 H3H

(56) Documents cited
GB A 2130829   GB 1516001   GB 1422127
GB 1107940   GB 1014727   EP A2 0078687
EP A1 0021650

(58) Field of search
H3H
Selected US specifications from IPC sub-classes
G03K H03M

(54) **Analogue to digital converter**

(57) A high resolution analogue to digital converter is provided, typically of 12 bit resolution, which has the speed of a full flash ADC but which has far fewer active components, typically 16 times less, and hence much lower power consumption. A coarse digital prediction 3 of the signal to be digitised is converted, DAC to analogue form and subtracted, 2, from the signal, 1. The difference, consisting of relatively few bits, is digitised, ADC, at speed and added, ADD, to the prediction, 5, to provide the full digitised signal 10. In many applications a prediction can be obtained from the immediate or longer term history of the signal. The input signal, 1, may be derived from an array of infra-red detectors viewing a scene.
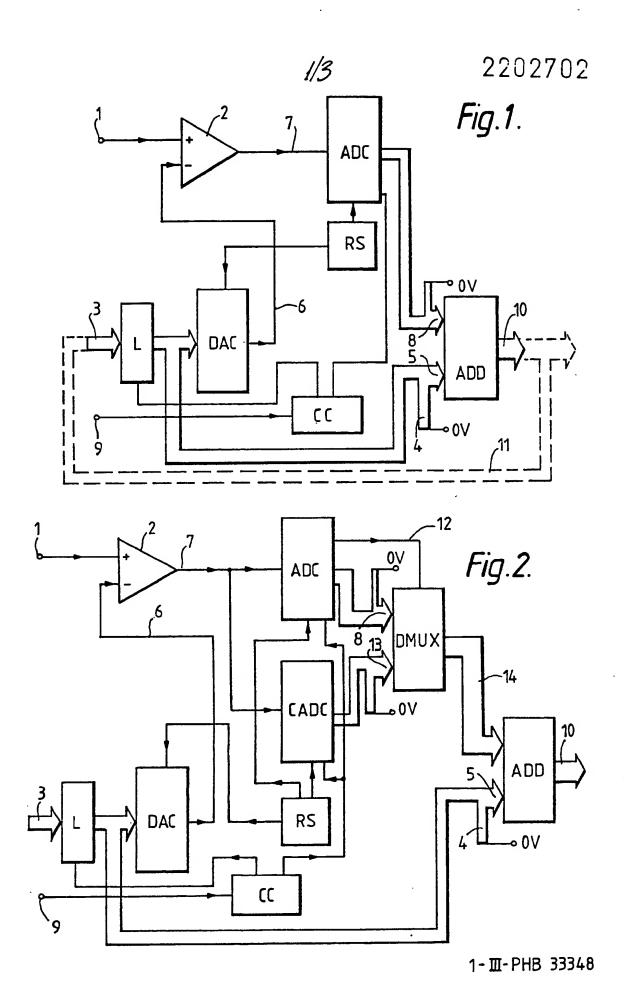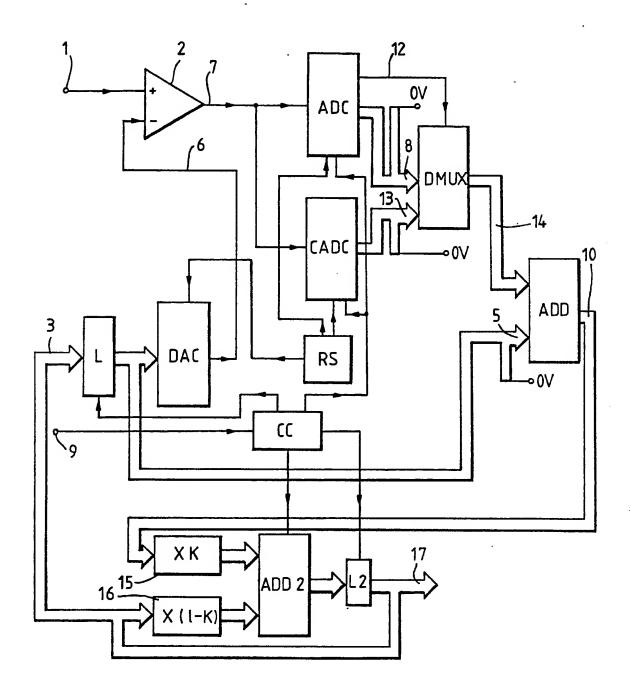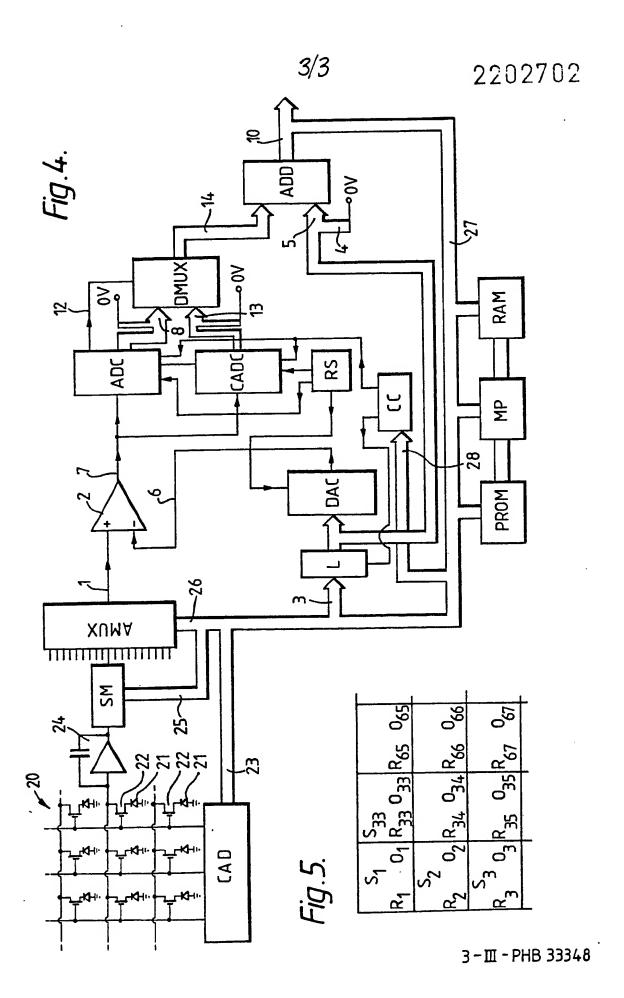

Fig.1.

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The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.

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Fig.1.

Fig.2.

Fig.3.

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Fig.4.

Fig.5.

		S_1 O_1		S_{33} O_{33}	R_{65} O_{65}
R_1		R_{33}			
		S_2 O_2		R_{34} O_{34}	R_{66} O_{66}
R_2					
		S_3 O_3		R_{35} O_{35}	R_{67} O_{67}
R_3		R_{35}			

DESCRIPTION

ANALOGUE TO DIGITAL CONVERTER

This invention relates to analogue to digital converters (ADC). More particularly it relates to analogue to digital converters of high resolution and/or high speed and low power consumption.

For the highest speeds the so-called "flash" converter is preferred. A flash converter compares an analogue input voltage simultaneously with all the voltages at the connections between a series-connected chain of equal resistors fed with a reference voltage. For a 10 bit ADC, for example, there are 1023 voltage comparators feeding a code converter with 1023 inputs (on/off) and a 10 bit binary coded output. While being fast, the area on a silicon chip can be excessive to accommodate the large number of comparators. The power consumption and hence the cooling requirements of such a converter are then also large. Tsukada et al, on page 34 of the Digest of Technical Papers of the 1985 IEEE International Solid-State Circuits Conference, disclose a CMOS 8 bit flash converter operating at 25M-Hz, i.e. a conversion cycle time of 40 nanoseconds. This converter has 2^8 i.e. 256 comparators and consumes 300 mW. If this approach were extended to a twelve bit converter, a resolution which will be seen to be realisable using the present invention, the number of comparators, and hence the power consumption, would need to be increased by a factor of 2^4, i.e. 16 times. Thus the silicon chip area would be increased by this factor and the power consumption would be about 4.8 watts, posing a serious cooling problem.

An approach to reducing the number of comparators is provided by the so-called "half-flash" converter, alternatively described as the "two-step flash" or "sub-ranging" converter. Half-flash ADC's are part of a broader family of multi-stage flash converters. In operation, each ADC stage generates a group of bits of the final output, starting with a group of the most significant bits (MSB) and working down the stages to the least significant group of bits (LSB), and subtracts the analogue value of that group of bits from

the input value to generate a residual signal which forms the input to the following stage. C.Ozdalga, on page 115 et seq. of Electronic Design, 6th February, 1986, discloses such a half-flash ADC, MP7685, having 11 bit resolution, 500ns conversion time, and a power dissipation of 100mW. A total of 96 comparators are employed, 32 to encode the 5 MSBs and 64 to encode the 6 LSBs, rather than the 2047 comparators that would be needed for a full flash 11 bit ADC.

A significant power reduction is achieved but at the expense of a conversion time which is more than 10 times longer than that of the flash converter described above.

Dhawan and Kondo, on pages 77 to 88 of IEEE Transactions on Nuclear Science, Vol 33, No 1, February, 1986, provide a review of recent progress in flash ADCs both full flash and half flash. A table is provided listing the salient features of 94 ADCs from most manufacturers, from which the trade-offs between resolution, speed and power consumption can be appreciated.

It is an object of the present invention to provide an ADC having a higher product of resolution and speed for a given power dissipation than that of presently available ADCs. The invention provides an analogue to digital converter for digitising an analogue input signal to a given resolution, characterised in that a digital to analogue converter is provided connected to receive a digital prediction of the analogue input signal and to output an analogue prediction of the analogue input signal, which analogue prediction has a stability and linearity at least equivalent to the given resolution, in that a difference amplifier is provided for forming an analogue difference signal between the analogue input signal and the analogue prediction, in that a first analogue to digital converter is provided for converting the analogue difference signal to a digital difference signal to the given resolution, and in that a digital adder is provided for adding the digital difference signal to the digital prediction to form a digital version of the analogue input signal at the given resolution.

The invention relies on the fact that, in many practical situations, an estimate or prediction of the analogue input signal can be obtained, either from the history of the signal itself or from other related signals. The shorter the time that has elapsed since the last digitisation of a continuously varying input signal, or the closer the relationship to another known signal, the closer can the prediction be to the actual new value of the input signal. The difference signal is then a smaller fraction of the input signal and so requires only a comparatively low resolution first ADC to provide the LSBs of the digitised signal. Such a first ADC can then be a full flash ADC with comparatively few comparators and hence low power consumption and yet have the highest speed of which a flash ADC is capable. The digital to analogue converter (DAC), by which the digital prediction is converted to the analogue prediction, can be constructed to operate at very high speeds since the digital input is applied in parallel to a transistor/resistor network. DACs can be 10 to 50 times as fast as an ADC of corresponding resolution and power consumption. Thus the analogue prediction can be available at the input to the difference amplifier in a very short time. Finally, the digital prediction and the digital difference signal are both available, in parallel, virtually simultaneously at the input to the digital adder, which can also be very fast.

The DAC can be of comparatively low resolution since it only handles the MSBs of the final digitised signal. But it must have a stability and linearity at least equivalent to the final resolution sought, otherwise gross errors in digitisation could occur when the prediction and difference are added.

In many cases an input signal has some dependence on its history or is related to other signals. The input may be the next part of a cyclical varying waveform which has been input for some time in the past. Thus the immediate past value can be known as can the rate of change of the immediate past value, from which a prediction can be formed. More simply, if the input waveform is sampled at sufficiently closely spaced intervals of time, the

immediate past value itself may be an acceptable prediction. The
analogue to digital converter in accordance with the invention may
be arranged to digitise a succession of samples of an analogue
input signal which varies continuously with time and may be
characterised in that a digital latch is provided connected to
receive the output of the digital adder and to store the digital
version of a sample of the analogue input signal, and in that the
output of the digital latch is connected to the input terminals of
the digital to analogue converter to provide the digital prediction
of a later sample of the analogue input signal.

The input signal may be the value of a picture element (pixel)
in, for example, a television picture or a thermal imaging
apparatus. The previous values of that pixel on previous frames can
be used to make the prediction. Also, the value of adjacent pixels
in the same frame may be used to make the prediction since they are
often of much the same value as the pixel concerned.

However, in practical situations the input analogue signal may
make a sudden large change in value immediately following a
digitisation. In the case of adjacent picture elements they may
differ markedly from one another.

In either event, the prediction will be seriously in error and
the difference signal will be beyond the range of the first ADC
resulting in a gross digitisation error when the prediction and
difference signal are added. To cope with this situation an
analogue to digital converter in accordance with the invention may
be characterised in that the first analogue to digital converter is
provided with means for generating an over range signal indicating
that the analogue difference signal is larger than the digitising
range of the first analogue to digital converter, in that a second
analogue to digital converter is provided for digitising the
analogue difference signal over a range of signal amplitudes
substantially equal to the range of the analogue input signal but
to a resolution coarser than the given resolution, and in that a
digital multiplexer is provided for selecting the output of the
second or the first analogue to digital converter for input to the

digital adder according as the over range signal is present or not respectively.

The effect is then that if the input and prediction do differ markedly, the input will be correctly digitised but to a coarser resolution than the given resolution. As soon as the difference between the prediction and the input falls inside the digitising range of the first ADC the digitised output is restored to the given resolution. Thus only at times of rapid change in a continuously varying analogue input signal or when adjacent picture elements differ widely as in the case of a scene having a bright point source in an otherwise dark background, for example, will there be any degradation of the digitised signal and only then as regards resolution. Fine detail in a waveform or scene which does not vary greatly in amplitude or brightness from the immediately prior waveform or background respectively will be digitised at the full given resolution.

When the analogue input signal is repetitive, successive digitisations of the signal may provide nominally equal values but which have a noise-like spread in their actual values. The invention may be employed to produce a more accurately defined value of the signal based upon an average of a number of samples. Alternatively expressed, the signal to noise ratio of the input signal may be improved. To this end, the invention may be adapted to digitise a repetitive analogue input signal, and may be characterised in that a digital recursive filter is provided, in that input terminals of the digital recursive filter are connected to receive the digital version of a repetition of the analogue input signal, and in that output terminals of the digital recursive filter, at which a filtered digital version of the repetitive analogue input signal is available, are connected to the input terminals of the digital to analogue converter to provide the digital prediction of a later repetition of the input signal.

A digital recursive filter, also known as an infinite impulse response filter (IIF) is an arrangement which can be used to provide a low-pass filter for a repetitive digital signal. In this

low-pass filter form of the IIF, a first fraction of a sample of a
digital input signal is added to a second fraction, equal to unity
minus the first fraction, of the previous digital signal value
output by the filter to produce a new output value from the
filter. After a number of samples of the digital signal have been
input, the output of the filter provides an average of all previous
inputs with diminishing weight for older samples.

In combination with apparatus in accordance with the
invention, the input to the IIF is the digitised output of the
adder of the analogue to digital converter and the output of the
IIF provides the digital prediction for input to the digital to
analogue converter as well as the final filtered output of the
analogue to digital converter. If the first fraction is K, then the
signal to noise ratio is improved by the factor $K^{-\frac{1}{2}}$. For example,
if K = 0.1, the improvement is approximately 3.2 times after some
30 or so samples.

The analogue to digital converter in accordance with the
invention may be arranged to digitise a succession of samples of an
analogue input signal which varies cyclically with time. A digital
latch is then provided connected to receive the output of the
digital adder and to store the digital version of a sample of the
analogue input signal. The output of the digital latch is connected
to the input terminals of the digital to analogue converter to
provide the digital prediction of a later sample of the analogue
input signal.

The analogue to digital converter in accordance with the
invention may also be arranged to digitise the analogue output
signals of an array of infra-red radiation detector elements having
known non-uniform responsivities to changes in incident infra-red
scene radiation and non-uniform offset signals in response to
standard incident infra-red radiation, a multiplexer being provided
for connecting the elements one at a time in turn to the analogue
to digital converter. Digital means are then provided for deriving
a digital prediction of the signal of a first element exposed to
incident scene radiation from the immediately previously digitised

signal of an adjacent second element also exposed to the incident
scene radiation, the digital means comprising means for storing
andaccessing the responsivities and offsets of all the elements in
the array and for storing and accessing the digitised output signal
of an element, means for subtracting the offset of the second
element from the digitised stored signal of the second element, and
means for adding the product to the offset of the first element to
produce the digital prediction for input to the digital to analogue
converter. The digital prediction is made on the assumption that
most adjacent pixels in an infrared scene imaged on the array have
nearly equal radiation intensities. Due allowance is then made for
the non-uniformities of the detectors in processing their outputs.

It should be noted that the non-uniform offset signals may
themselves be determined with improved signal to noise ratio, as
mentioned above, by applying the standard incident infrared
radiation to each detector and using the digital recursive filter
as described above. The advantage is then obtained that the offsets
contribute much reduced noise to the digitised element signals.

Embodiments of the invention will now be described, by way of
example, with reference to the accompanying drawings in which,

Figure 1 shows an analogue to digital converter in accordance
with the invention,

Figure 2 shows an analogue to digital converter having means
for accepting an input signal which differs markedly from the
predicted input signal,

Figure 3 shows an analogue to digital converter for digitising
a repetitive input signal with improved signal to noise ratio.

Figure 4 shows an analogue to digital converter arranged to
digitise the output signals of a two dimensional array of infrared
radiation detectors, and

Figure 5 shows schematically part of an array of store
locations for the responses and offsets of the detector array of
Figure 4.

Figure 1 shows an embodiment of a basic analogue to digital
converter in accordance with the invention. An analogue input

signal to be digitised to an accuracy of 1 part in 4096, i.e. 1 part in 2^{12}, is applied to terminal 1 of a difference amplifier2. A digital prediction of the input signal is applied to the six binary lines of an input 3, shown as a broad arrow, of a

5   digital latch L. The digital prediction, derived from a source not shown, is of the six most significant bits of the final 12 bit digitised output. The lowest order bit of the prediction has a significance 64 times larger, i.e. 2^6, than the lowest order bit of the final digitised output. Latch L stores the digital

10   prediction and inputs it to a 6 bit digital to analogue converter DAC and to a 12 bit adder ADD as the 12 bit number XXXXXX000000, X indicating a digit, 0 or 1, of the prediction and the six 0's being indicated as the six 0 volt inputs of the lower half 4 of the broad arrow 12 bit prediction input 5 to ADD.

15   DAC converts the digital prediction into an analogue prediction at high speed. For example, DAC may use binary-weighted current mirrors which are switched selectively into an output resistor. Alternatively, DAC may consist of a series chain of resistors fed from a d.c. reference source RS. The resistors are

20   proportioned so that the tappings on the chain supply d.c. voltages with respect to earth which increase by a factor of two at each step up the chain. High speed switches are provided at each of the six tapping points, the switches being simultaneously controlled one each by the six binary digit inputs from L. The selected

25   tapping voltages are added together by an analogue adder, either comprising a high gain d.c. fed-back amplifier with six inputs, or a current adding node of a resistor network. The resistor chain and switches have a stability and linearity at least equivalent to the final 12 bit resolution. Thus, a change of one digit in the

30   prediction, at any point in the prediction range, will always produce a voltage output change from DAC closely equal to 64 times a voltage change on the input signal corresponding to a one digit change in the least significant bit of the final output.

The difference amplifier 2 subtracts the analogue prediction

35   output on connection 6 by DAC from the analogue input signal. The

subtraction is made to an accuracy better than 1 part in 4096 so
that the analogue difference signal output on connection 7 has an
accuracy at least equal to the least significant bit in the final
digitised output. The analogue difference signal is applied to an
analogue to digital converter ADC which has an 8 bit dynamic
range. For highest speed, ADC will be a flash converter, but it
could be a half-flash converter or any other design which gives a
sufficiently short conversion time for an application envisaged. In
any event a voltage reference source is required in ADC and this is
also supplied from the reference source RS so that the voltage
references of DAC and ADC are tied together, preventing
digitisation errors due to relative drift of reference sources.

The digitised difference signal is output by ADC and is
combined with four most significant bit zeros to form a 12 bit
number OOOOXXXXXXXX, X indicating a digit of the difference signal
and the four O's being indicated as the four O volt inputs to the
upper third of the broad arrow 12 bit difference input 8 to ADD.
The reference source RS is set up initially so that a change in the
least significant bit only of the digital prediction held in L
produces, via DAC, difference amplifier 2 and ADC a change in only
the seventh bit output by ADC, the six bits of lower significance
being undisturbed. The seventh and eighth bits of ADC output are
added so that, provided the prediction is within 6% i.e. 1/16th of
the dynamic range of the final 12 bit output, the analogue
difference signal will be within the range of ADC. The difference
amplifier 2 must have a common mode rejection of at least 24db to
preserve accuracy but need not have good large signal slew
characteristics. The speed of response of difference amplifier 2 to
changes in input or prediction is chosen to suit the particular
application envisaged.

The addition of the digitised prediction and the digitised
difference signal in ADD and output on terminal 10 may be depicted
as follows.

	MSB	LSB
Prediction	X X X X X X 0 0 0 0 0 0	
Difference	0 0 0 0 X X X X X X X X	

X X X X X X X X X X X X

It should be noted that, in use within the design range of the analogue to digital converter, the prediction and difference do not add up to 13 digits but always to 12 digits or less.

A control circuit CC is provided which, in response to a timing input signal on terminal 9, provides appropriately timed signals to latch L and ADC. The latch L samples and holds the prediction input for the digitisation period and ADC is timed to digitise the difference signal at the correct instant.

In the event that the analogue input is changing slowly relative to the time between digitisations, a preceding digitised output signal on output 10 can be fed to latch L to act as the prediction for the next digitisation. Only the six most significant bits of the output at 10 are fed back and the connection 11 from output 10 to latch L is shown dotted. In this event the timing of the control circuit CC is adjusted to store these six digits in L from one digitisation period to the next.

In the event that the prediction and the input signal differ by more than 6 per cent, ADC will be taken out of its 8 bit range, any higher order bits of the digital difference signal being lost. When the addition is made in ADD a gross error in output 10 will occur. Figure 2 shows an analogue to digital converter in accordance with the invention modified to overcome this problem. All the circuit units of Figure 1 are present in Figure 2 and are numbered or indicated in the same way. However, in addition a coarse analogue to digital converter CADC is provided to which the analogue difference signal is also fed. CADC is also fed from the same reference voltage source RS to ensure relative stability. In this embodiment CADC is a 6 bit flash converter operating over the full range of the analogue input signal. Thus even if the prediction is zero but the input signal is at maximum, CADC will

digitise the input signal to 6 bit accuracy. ADC is provided with a
binary over-range output on connection 12 which is present when a
ninth or higher order bit is present in ADC output. As in Figure 1
ADC output is made up to a 12 bit number on connection 8. CADC only
provides the six MSB's of the difference signal and is made up to a
12 bit number by the addition of 6 zeros as LSB's on connection
13. ADC and CADC outputs are fed to a 12 bit digital multiplexer
DMUX which selects either CADC output or ADC output according as
the over-range output is present on connection 12 or not
respectively. The DMUX output 14 is fed to the digital adder ADD to
produce the final digital output. In the event of an over-range
indication, the inputs to ADD appear as follows.

	MSB										LSB
Prediction	X	X	X	X	X	X	0	0	0	0	0	0
Difference	X	X	X	X	X	X	0	0	0	0	0	0

X	X	X	X	X	X	0	0	0	0	0	0

Thus, a full range digitisation of the input signal is
provided to a lower, 6 bit, resolution. As soon as the input and
prediction differ by less than 6 per cent, the over-range
indication disappears and a full resolution digitisation is
provided.

The analogue to digital converter of Figure 2 may appear
complex. But it should be noted that the number of circuit units is
12 for DAC, 2^6 for CADC, and 2^8 for ADC, making a total of
332. This is to be compared with $2^{12} = 4096$ for a full flash 12
bit ADC.

The analogue input signal may be repetitive, successive
digitisations of the signal providing nominally equal values but
which have a noise-like spread in their actual values.

Figure 3 shows the embodiment of the invention of Figure 2
modified by the inclusion of a digital recursive filter in such a
manner as to provide the value of a repetitive input signal with
improved signal to noise ratio. The filter comprises digital
multipliers 15 and 16 for multiplying digital input signals by

factors K and (1-K) respectively, where K is a number less than unity, a digital adder ADD2 for adding the factored signals together, and a digital latch L2 for storing the sum of the factored signals.

5   The digitised input signal on connection 10 is fed to multiplier 15. The contents of latch L2, which ultimately provide the filtered output 17, are fed to the multipler 16 and also to latch L to provide the prediction of the input signal. Initially, before the repetitive signal commences, the contents of latch L2
10   are zero and the prediction is therefore zero. With the first sample of a non-zero input signal at terminal 1, ADC will almost certainly be out of range and DMUX will select the output of CADC. Output 10 will hence carry the full signal digitised to coarse resolution. Under the control of timing signals from CC, ADD2
15   passes K times output 10 to L2 where it is stored for use as the prediction for the next sample of the input signal at terminal 1 and also forms the first output value at 17. CC receives its timing input on terminal 9 from an input signal sampling device, not shown.

20   As an example, a normalised, or unity, repetitive input and K = 0.2 will be assumed. The following table gives the succession of outputs 17 obtained.

SAMPLING INSTANT	FILTERED OUTPUT	
0	0.2	
1	0.2 + (o.8 x 0.2) = 0.36	
2	0.2 + (o.8 x 0.36) = 0.488	
3	0.2 + (0.8 x 0.488) = 0.5904	
:	:	
:	:	
8	0.2 + (=.8 x 0.83) = 0.866	:
:	:	:
:	:	:
12	:	0.945
:		:
:		:
20		.991

It will be seen that after 12 samples, the output is within 6%
of the input. ADC is then in range and the output 10 will change to
a full resolution output. After 20 samples the output is within 1%
of the input at high resolution. With further samples the output
will approach an average of the input, taking into account earlier
samples with lower weight. The output 17 will still fluctuate, but
to a smaller extent than input 1. The effective reduction in noise
is given by the factor $K^{-\frac{1}{2}}$. In the foregoing example with
$K = 0.2$, the noise reduction factor is 2.236, and the average
output signal is obtained after some 20 to 25 samples. Smaller
values of K will produce better noise reduction but will require
more samples of the input.

Figure 4 shows an example of the invention applied to
digitising the signals arising from an array of picture elements.
The prediction of the signal of one picture element is obtained by
assuming that the brightness of that picture element is nearly the
same as that of an adjacent picture element whose signal has
previously been digitised. In the example, the signals arise from
an array of infrared detectors upon which an infra-red image of a
natural scene has been focused. It is characterisitic of natural
infrared scenes that, within any large area of land or grass or
water surface, much the same temperature and emissivity frequently
occur. If such an area is focused on an array of infra-red equal,
provided due allowance is made for the differing responsivities of
the detectors in the array and also for the differing offset
signals obtained when all detectors are exposed to a standard
reference radiation intensity.

Figure 4 shows a small part 20 of a rectangular
two-dimensional staring array of cadmium mercury telluride (CMT)
photovoltaic detectors 21. The detectors are arranged in rows and
columns, each detector being sampled by an MOS switch 22. The
columns of detectors are sampled, one at a time, by a column
address decoder CAD, in response to a digital column address
supplied on input 23. The outputs of each row of detectors are
connected in parallel to a separate integrator 24 and sample and

hold circuit SH (only one being shown) and thence to the inputs of
an analogue multiplexer AMUX, which, in response to a digital row
address supplied on input 26 connects any one SH output to
connection 1. Thus, in response to a column and row address, the

5   integrated output of any one detector 21 can be applied as an input
signal on connection 1 to the over-range capability analogue to
digital converter described with reference to Figure 2. This type
of converter is preferred in this application since it is another
characteristic of natural infrared scenes that small but intense

10   sources of infrared radiation can be present due to live animals,
fires and man-made sources such as vehicle exhausts and recently
used weapons. Thus an occasional small group of picture elements
may differ sharply from their neighbours. A low resolution
digitisation of picture elements at the boundaries of such groups

15   is often entirely acceptable. Also, later picture elements in the
same group may be digitised to high resolution. Accurate
digitisation of infra-red scenes is of interest since digital
computations can then be carried out on sub-sets of picture element
signals to seek for target features.

20   As mentioned above, allowance must be made for the differing
responsivities and offsets of the detectors. Responsivity, in volts
of signal per watt of radiation incident upon the detector, will be
indicated herein by R_n for the nth detector in the array. The
offset signal, in volts, from a detector upon which a standard

25   reference infra-red radiation is incident will be indicated by O_n,
the signal voltage from the scene being indicated by S_n for the nth
detector. If the scene radiations incident upon two adjacent
detectors n and (n-1) are assumed to be the same, this canbe
expressed as

30
$$\frac{S_n - O_n}{R_n} = \frac{S_{n-1} - O_{n-1}}{R_{n-1}}$$

from which S_{np}, the signal prediction for the nth detector, is
given by

35

$$S_{np} = R_n \frac{(S_{n-1} - O_{n-1}) + O_n}{R_n - 1} \text{---I}$$

Thus, if the responsivities and offsets of all the
detectors in the array have been previously determined and stored,
then predictions can be made for each detector signal in turn once
the signal of the first detector has been digitised, at coarse
resolution from a zero prediction, by the analogue to digital
converter of the invention. At each digitisation, the actual value
of the signal, at coarse or fine resolution, of the detector
concerned will be obtained, stored and used to make the next
prediction. Figure 5 schematically indicates part of a random
access store of information for a square array of 32 x 32
detectors. All responsivities R and offsets O are shown stored, the
actual signal S_{33} having just been determined and S_{34} about to be
determined using S_{33} as a prediction.

Figure 4 shows a microprocessor MP and associated random
access memory RAM and a programmable read only memory PROM
programmed to carry out the calculation of Equation I above, and to
time the operations needed for each digitisation. A data bus 27 is
connected to convey each digitised signal Sn from output 10 to RAM
where it is stored associated with R_n and O_n as indicated in Figure
5. The programme in PROM is then acted upon by MP and the
prediction for the next picture element is output on the data bus
to input 3 of latch L. From data stored in PROM, MP also calculates
the succession of row and column address, outputs them on the data
bus to inputs 26 of AMUX and 23 of CAD respectively. Data bus 25
connected to all the SH circuits provides timing signals to reset
each integrator to zero and release stored data in each SH in
preparation for the next detector signal. Likewise the control
circuit CC of the analogue to digital converter receives timing
signals on input 28 from the data bus.

In a typical system the digital recursive filter feature
described with reference to Figure 3 may be incorporated in the
analogue to digital converter and used in a preliminary operation

to determine the responsivities and offsets with reduced noise. For
the offsets a standard reference radiation is arranged, by means
not shown, to fall upon each detector. The detector output is then
sampled repetitively to determine the offset with reduced noise,
the result then being stored in RAM. For the responsivities, a
standard increment of radiation, above the reference, is then
arranged to fall on each detector and the detector output sampled
repetitively. The associated offset is then subtracted from the
filtered detector output, the result being stored in RAM as the
responsivity associated with the offset. Alternatively, if the
characteristics of the infrared detector array are known to be
stable, the array can be calibrated and all offset and responsivity
coefficients programmed into a separate PROM to which MP has
access.

CLAIMS

1. An analogue to digital converter for digitising an analogue input signal to a given resolution, characterised in that a digital to analogue converter is provided connected to receive a digital prediction of the analogue input signal and to output an analogue prediction of the analogue input signal, which analogue prediction has a stability and linearity at least equivalent to the given resolution, in that a difference amplifier is provided for forming an analogue difference signal between the analogue input signal and the analogue prediction, in that a first analogue to digital converter is provided for converting the analogue difference signal to a digital difference signal to the given resolution, and in that a digital adder is provided for adding the digital difference signal to the digital prediction to form a digital version of the analogue input signal at the given resolution.

2. An analogue to digital converter as claimed in claim 1 characterised in that the first analogue to digital converter is provided with means for generating an over range signal indicating that the analogue difference signal is larger than the digitising range of the first analogue to digital converter, in that a second analogue to digital converter is provided for digitising the analogue difference signal over a range of signal amplitudes substantially equal to the range of the analogue input signal but to a resolution coarser than the given resolution, and in that a digital multiplexer is provided for selecting the output of the second or the first analogue to digital converter for input to the digital adder according as the over range signal is present or not respectively.

3. An analogue to digital converter as claimed in Claim 1 or Claim 2 adapted to digitise a repetitive analogue input signal, characterised in that a digital recursive filter is provided, in that input terminals of the digital recursive filter are connected to receive the digital version of a repetition of the analogue input signal, and in that output terminals of the digital recursive filter, at which a filtered digital version of the repetitive

analogue input signal is available, are connected to the input
terminals of the digital to analogue converter to provide the
digital prediction of a later repetition of the input signal.

4. An analogue to digital converter as claimed in claim 1 or
claim 2, arranged to digitise a succession of samples of an
analogue input signal which varies cyclically with time
characterised in that a digital latch is provided connected to
receive the output of the digital adder and to store the digital
version of a sample of the analogue input signal, and in that the
output of the digital latch is connected to the input terminals of
the digital to analogue converter to provide the digital prediction
of a later sample of the analogue input signal.

5. An analogue to digital converter as claimed in Claim 1 or
Claim 2 arranged to digitise the analogue output signals of an
array of infrared radiation detector elements having known
non-uniform responsivities to changes in incident infrared scene
radiation and non-uniform offset signals in response to standard
incident infrared radiation, a multiplexer being provided for
connecting the elements one at a time in turn to the analogue to
digital converter, characterised in that digital means are provided
for deriving a digital prediction of the signal of a first element
exposed to incident scene radiation from the immediately previously
digitised signal of an adjacent second element also exposed to the
incident scene radiation, the digital means comprising means for
storing and accessing the responsivities and offsets of all the
elements in the array and for storing and accessing the digitised
output signal of an element, means for subtracting the offset of
the second element from the digitised stored signal of the second
element, means for multiplying the remainder by the ratio of the
responsivity of the first element to the responsivity of the second
element, and means for adding the product to the offset of the
first element to produce the digital prediction for input to the
digital to analogue converter.

6. An analogue to digital converter substantially as described
with reference to any one of Figures 1, 2 or 3, or Figures 4 and 5.